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EXAMINER	
VU, TRISHA U	
ART UNIT	**PAPER NUMBER**
2112	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/385,978	LEE ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed 03-18-04* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 31-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *42* is/are allowed.

6)☒ Claim(s) *1-29,31-41 and 43-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-29 and 31-45 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Tomizawa et al. (6,202,082) (herein after Tomizawa).

As to claim 1, James teaches a method of communicating between a plurality of functional blocks comprising: originating a packet (by a producer); passing the packet (each node is capable of passing by any packets that are not targeted for that node) (col. 5, lines 6-10). However, James does not explicitly disclose decoding the packet to extract configuration information from the packet and utilizing the configuration information to configure one of the plurality of functional blocks. Tomizawa teaches decoding configuration information packets to extract configuration information from the packet and utilizing the configuration information to configure one of the plurality of nodes (col. 20, lines 36-53, col. 22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of James to allow each node to

know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

As to claim 2, James further teaches originating is performed by a master (producer) (col. 2, lines 10-14).

As to claims 3, 4, James further teaches passing is performed by a first target, and decoding is performed by a first target (col. 5, lines 5-10 wherein multicast and broadcast packets imply that a first target receives/decodes the packet and passes the packet to other targeted nodes).

As to claims 5, 6, James further teaches decoding is performed by a second target, and passing is performed by the second target (col. 5, lines 5-10 wherein multicast and broadcast packets imply that a second target receives/decodes the packet and passes the packet to other targeted nodes).

As to claim 7, James further teaches utilizing is performed by the second target (col. 2, lines 3-15) and passing is performed by the second target (col. 25, lines 5-10 wherein multicast and broadcast packets imply that the second target passes the packet to other targeted nodes).

As to claim 8, James further teaches removing the packet (aged packets are discarded when they pass through the scrubber) (col. 6, lines 23-26).

As to claim 9, James further teaches the first target comprising a ring interface and a control, the second target comprising a ring interface and a control, the master comprising a ring interface and a control, a ring connecting to the ring interface of the first target, the ring interface of the second target, and the ring interface of the master in a daisy chain fashion,

the ring used for the passing and the originating (Figs. 4, 5, 7 for interface connection between the nodes wherein node1 can be the first master and subsequent nodes can be targets, and col. 9, lines 17-21 wherein a control in each of the nodes can be at least a transmit unit 250 and/or a receive unit 252 with scrubber 218).

As to claim 10, James further teaches the master performing the removing after the passing brings the packet back to the master (col. 6, lines 23-26 and col. 40-44 wherein a scrubber for removing aged packets preferably is available within all of the nodes, and thus it can be implemented at the master node).

As to claim 17, James teaches a communications network comprising: a first master having a ring interface and a control; a first target having a ring interface and a first decoder; a first ring connection coupling the ring interface of the first master to the ring interface of the first target; a second target having a ring interface and a second decoder; and a second ring connection coupling the ring interface of the first target to the ring interface of the second target to pass a first plurality of packets; and a third ring connection coupling the ring interface of the second target to the ring interface of the first master to pass a second plurality of packets (Figs. 4, 5, 7 for interface connection between the nodes wherein node1 can be the first master and subsequent nodes can be targets, and col. 9, lines 17-21 wherein a control in each of the nodes can be at least a transmit unit 250 and/or a receive unit 252 with scrubber 218). However, James does not explicitly disclose configuration information packets to configure the nodes. Tomizawa teaches configuration information packets to configure nodes (col. 20, lines 36-53, col. 22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of James to

allow each node to know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

As to claim 18, James further teaches the master originates the plurality of packets which are passed via the first ring connection to the first target (each node is capable of passing by any packets that are not targeted for that node) (col. 5, lines 6-10).

As to claim 19, James further teaches the first target passed the plurality of packets via the second ring connection to the second target; and the second target passes the set of packets via the third ring connection to the first master (each node is capable of passing by any packets that are not targeted for that node) (col. 5, lines 6-10).

3. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Tomizawa et al. (6,202,082) (herein after Tomizawa), and further in view of Williams et al. (6,167,480) (hereinafter Williams).

As to claim 20, the argument above for claim 19 applies. However, James and Tomizawa do not explicitly teach the first target on an integrated circuit; and the second target on the integrated circuit. Williams teaches a combination of devices can be implemented as a single integrated circuit or a set of integrated circuits (col. 8, lines 26-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first target on an integrated circuit; and the second target on the integrated circuit as taught by Williams in the system of James and Tomizawa because integrated circuits provide high speed communication and a flexible compact design as desired by user.

4. Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Tomizawa et al. (6,202,082) (herein after Tomizawa) as applied to claim 1 above, and further in view of Christiansen et al. (5,983,302) (herein after Christiansen).

As to claim 11, James further teaches a ring used for the originating and the passing (col. 3, lines 5-10). However, James and Tomizawa do not explicitly disclose requesting the ring and granting the ring. Christiansen further teaches requesting and granting a shared bus (col. 5, lines 26-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include requesting and granting the shared bus as taught by Christiansen in the ring system of James and Tomizawa to provide a computer system wherein the control of a shared bus by a plurality of devices include in the computer system is provided in a manner whereby overall operating efficiency is enhanced without effectively denying one or more devices in the computer system form control of the bus for extended periods of time (col. 2, lines 49-54).

As to claim 12, James further teaches the originating is performed by a first master (col. 2, lines 10-14).

As to claim 13, Christiansen further teaches the requesting is performed by a second master (col. 5, lines 34-56).

As to claim 14, Christiansen further teaches the granting is performed by the first master (by arbiter 22) (col. 5, lines 17-33 wherein arbiter 22 can be located anywhere throughout the computer system, thus it can be located as part of a first master device).

As to claim 15, Christiansen further teaches the granting is performed by an arbiter (by arbiter 22) (col. 5, lines 17-33).

As to claim 16, Christiansen further teaches arbitrating between a first master requesting the ring and a second master requesting the ring (col. 5, lines 50-56).

5. Claims 21-25, 27-29, 31-35, 37, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen) and PCI Local Bus Specification (Herein after PCI Spec), and further in view of in view of Tomizawa et al. (6,202,082) (herein after Tomizawa).

As to claim 21, James teaches a communications network comprising: a first master; a first target; a second target; and a ring coupled to the first master, the first target, the second target (Figs. 4, 5 for ring connection between the nodes wherein node1 can be the first master and subsequent nodes can be targets). However, James does not explicitly disclose the ring comprising a packet valid line configured to indicate whether a valid packet is being transmitted on the ring. Christiansen teaches a packet valid line (FRAME# line) configured to indicate whether a valid packet is being transmitted on the ring (note Fig. 2 wherein a PCI local bus is provided for transmitting data between requesting devices, thus FRAME# line is inherent in PCI local bus). PCI Spec is being provided as evidence that a PCI local bus comprises a FRAME# line. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include PCI local bus with a packet valid line as taught by Christiansen in the ring system of James because PCI bus provides high communication speed. However, James and Christiansen do not explicitly disclose configuration information packets to configure the nodes. Tomizawa teaches configuration

information packets to configure nodes (col. 20, lines 36-53, col. 22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of James and Christiansen to allow each node to know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

As to claim 22, James further teaches a second master, the ring coupled to the second master (Figs. 4, 5 and col. 5, lines 5-10 wherein node1 can be the first master and one of the subsequent nodes can be the second master).

As to claim 23, James does not explicitly disclose an arbitrator, the arbitrator coupled to the first mater, the arbitrator coupled to the second master, the arbitrator controlling activity of the first master and the second master. Christiansen teaches an arbitrator coupled to requesting devices, the arbitrator controlling activity of the requesting devices (col. 5, lines 26-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an arbitrator coupling to the requesting devices and controlling the activity of requesting devices as taught by Christiansen in the ring system of James to provide a computer system wherein the control of a shared bus by a plurality of devices include in the computer system is provided in a manner whereby overall operating efficiency is enhanced without effectively denying one or more devices in the computer system form control of the bus for extended periods of time (col. 2, lines 49-54).

As to claim 24, Christiansen further teaches a request line (request line 28), the request line coupled to the first master, the request line coupled to the second master

(requesting devices); and a grant line (grant line 30), the grant line coupled to the first master, the grant line coupled to the second master (Fig. 2).

As to claim 25, Christiansen further teaches the request line configured to pass signals in a first direction, the grant line configured to pass signals in a second direction (Fig. 2).

As to claim 27, James does not explicitly disclose a request line, the request line coupled to the first master, the request line coupled to the second master, the request line coupled to the first target, the request line coupled to the second target. Christiansen teaches a request line coupled to requesting devices (col. 5, lines 26-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a request line coupling to the requesting devices as taught by Christiansen in the ring system of James to provide a computer system wherein the control of a shared bus by a plurality of devices include in the computer system is provided in a manner whereby overall operating efficiency is enhanced without effectively denying one or more devices in the computer system form control of the bus for extended periods of time (col. 2, lines 49-54).

As to claim 28, Christiansen further teaches the request line configured such that signals flow in a logically opposite direction to signals on the ring (Fig. 2).

As to claim 29, James further teaches a set of data lines configured to transmit signals (bus to transmit packet) (col. 2, lines 7-11). However, James does not explicitly teach a grant line. Christiansen further teaches a grant line configured to indicate a master may use the ring (grant line 30) (Fig. 2).

As to claim 31, James further teaches the ring comprising a set of data lines, the data lines configured to transmit signals (bus to transmit packet) (col. 2, lines 7-11).

As to claim 32, James further teaches the first master utilizing the ring to transmit signals to the first target, the first target utilizing the ring to transmit signals to the second target, the second target utilizing the ring to transmit signals to the first master (col. 5, lines 1-9).

As to claim 33, James further teaches the first master comprising a ring interface coupled to the ring and a control coupled to the ring interface, the control suitable for generating packets, the packets transmitted through the ring interface to become signals on the ring (Figs. 4, 5, 7 for interface connection between the nodes, and col. 8, lines 34-54 wherein the control can be at least a transmit unit 250).

As to claim 34, James further teaches the first target comprising a ring interface and a decoder coupled to the ring interface, the decoder receiving the signals that represent a packet (receive unit 252) (Figs. 4, 5, 7 for interface connection between the nodes), the decoder determining if the packet is addressed to the first target (by TargetID field 92 of the packet as shown in Fig. 2).

As to claim 35, James further teaches the second target comprising a ring interface and a decoder coupled to the ring interface, the decoder receiving the signals that represent a packet (receive unit 252) (Figs. 4, 5, 7 for interface connection between the nodes), the decoder determining if the packet is addressed to the second target (by TargetID field 92 of the packet as shown in Fig. 2).

As to claim 37, James further teaches the packet comprised of a fixed number of units of data, the units of data encoding an address (TargetID and/or SourceID) (col. 1, lines 41-44 and col. 5, lines 51-64).

As to claim 41, James further teaches the second master comprising a buffer (elasticity buffers 222 and 224), the buffer utilized for storing incoming data when the second master originates a packet, the incoming data passed after the second master completes origination of the packet (Fig. 7 and col. 8, lines 34-45).

1. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen) and PCI Local Bus Specification (Herein after PCI Spec), further in view of Tomizawa et al. (6,202,082) (herein after Tomizawa) as applied to claim 25 above, and further in view of Desyllas et al. (4,697,268) (herein after Desyllas).

As to claim 26, James, Christiansen and Tomizawa do not explicitly teach the first direction and the second direction dynamically alterable. Desyllas teaches bus request/grant directions are dynamically alterable (col. 2, lines 38-50 wherein bus request/grant lines are bi-directional lines for carrying request and grant signals in opposite direction, this implies that opposite directions are dynamically alterable since the lines are bi-directional lines). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bi-directional request/grant lines (dynamically alterable request/grant directions) as taught by Desyllas in the system of James, Christiansen and Tomizawa to provide alternate path for data transmission and thus improve the system's speed.

2. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen) and PCI Local Bus Specification (Herein after PCI Spec), further in view Tomizawa

et al. (6,202,082) (herein after Tomizawa) as applied to claim 35 above, and further in view of Hartmann et al. (6,047,002).

As to claim 36, James further teaches the packet comprised of a header and a set of data (Fig. 2 and col. 12, lines 46-67). However, James does not explicitly teach the header including an indication of the logical size of the set of data. Hartmann teaches a header including an indication of the logical size of the set of data (data length field (col. 11, lines 50-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a header including an indication of the logical size of the set of data as taught by Hartmann in the system of James, Christiansen and Tomizawa to provide the system with the ability to transmit packets of different sizes wherein the data size field helps the receive unit to better utilize its buffer to store data.

6. Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen), PCI Local Bus Specification (Herein after PCI Spec), Tomizawa et al. (6,202,082) (herein after Tomizawa) as applied to claim 21 above, and further in view of Williams et al. (6,167,480) (hereinafter Williams).

As to claim 38, James does not explicitly teach the first master, the first target and the second target on an integrated circuit. Williams teaches a combination of devices can be implemented as a single integrated circuit or a set of integrated circuits (col. 8, lines 26-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first master, the first target and the second target on an integrated circuit or a set of integrated circuits as taught by Williams in the system of James,

Christiansen, PCI Spec, and Tomizawa because integrated circuits provide high speed communication and a flexible compact design as desired by user.

As to claim 39, James does not explicitly teach the first master and the first target on a first integrated circuit, the second target on a second integrated circuit. Williams teaches a combination of devices can be implemented as a single integrated circuit or a set of integrated circuits (col. 8, lines 26-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first master and the first target on a first integrated circuit, the second target on a second integrated circuit as taught by Williams in the system of James, Christiansen, PCI Spec, and Tomizawa because integrated circuits provide high speed communication and a flexible compact design as desired by user.

As to claim 40, James does not explicitly teach the first master on a first integrated circuit, the first target and the second target on a second integrated circuit. Williams teaches a combination of devices can be implemented as a single integrated circuit or a set of integrated circuits (col. 8, lines 26-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first master on a first integrated circuit, the first target and the second target on a second integrated circuit as taught by Williams in the system of James, Christiansen, PCI Spec, and Tomizawa because integrated circuits provide high speed communication and a flexible compact design as desired by user.

7. Claims 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (6,275,885) (hereinafter Chin) in view of Williams et al. (6,167,480) (hereinafter Williams).

As to claim 43, Chin teaches a system comprising: a graphics memory device (frame buffer 24 and/or system memory 18); an accelerated graphics port (20); and a graphics expander bridge (bus interface unit 14)coupled to the graphics memory device and the accelerated graphics port (Fig. 1), the graphic expander bridge comprising a plurality of functional blocks (PCI Controller 40, AGP Controller 46, and other devices) and a ring by which the plurality of functional blocks are coupled to each other (Fig. 2), each of the plurality of functional blocks having a decoder and a plurality configuration registers (col. 10, lines 5967 and col. 11, lines 1-7), wherein one of the plurality of functional blocks originates one or more packets containing configuration information and passes the one or more packets to one or more of the remaining functional blocks via ring to configure the one or more of the remaining function blocks (col. 6, lines 22-67). However, Chin does not explicitly disclose the ring and the plurality of functional blocks residing on a single integrated circuit chip. Williams teaches a combination of devices can be implemented as a single integrated circuit or a set of integrated circuits (col. 8, lines 26-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to the ring and the plurality of functional blocks residing on a single integrated circuit chip as taught by Williams in the system Chin because integrated circuits provide high speed communication and a flexible compact design as desired by user.

As to claim 44, Chin further teaches each of the plurality of functional blocks further comprises a ring interface to coupled to the ring (Fig. 2 and col. 6, lines 22-57).

As to claim 45, Chin further teaches the ring comprises a plurality of data lines to transmit the one or more packets (Fig. 2 and col. 6, lines 22-57).

Response to Arguments

With respect to Applicant's argument on pages 12-13 of the Remarks that "*Tomizawa still fails to disclose utilizing the configuration information* ***to configure one of the plurality of functional blocks*** *because Tomizawa merely discloses a "****ring configuration*** *information packet"*, it is noted that Tomizawa teaches the nodes collect **information relating to the network configuration of node deployment and conditions of nodes** in each ring" (at least col. 18, lines 43-56), therefore this information is interpreted as configuration information to configure one of the plurality of functional blocks (nodes) because the nodes use this information in order to operate accordingly and appropriately.

Applicant's arguments with respect to claim 42 on pages 14-15 of the Remarks have been fully considered and are persuasive. The rejection of claim 42 has been withdrawn.

Allowable Subject Matter

8. Claim 42 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 42 includes the limitation of the address chip including a configuration ring having a master, a first target, and a second target, wherein the master originates a plurality of packets containing configuration information and passes the plurality of packets via the ring to configure the first and second targets, which is not shown by the prior art of record, in the combination as disclosed and claimed. The examiner interpreted the claim in light of the specification and in view of Applicant's persuasive argument that "the address compass logic 10 in Szczepanek, which is within the LAN adapter 4, does not include a configuration ring" (page 15 of the Remarks).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses AGP system and data/address chips:

US Patent	6,363,439	Battles et al.
US Patent	6,330,654	LaBerge et al.
US Patent	6,564,241	Rosengard
US Patent	5,829,016	Sharma et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER